WHAT IS CLAIMED IS:

1. A semiconductor device manufacturing method comprising:

a first step of introducing impurities into a surface layer in an active region of a semiconductor substrate and annealing said semiconductor substrate to form source and drain regions;

after said first step, a second step of forming a multilayer film so as to cover said active region, said multilayer film being made up from at least three layers, in which a first insulating film having a charge trap function is sandwiched by second and third insulating films from upper and lower sides of said first insulating film; and

a third step of depositing an electrode material on said multilayer film and patterning said electrode material and said multilayer film to form a gate electrode, said gate electrode being located over said semiconductor substrate with said multilayer film being interposed between them.

2. The method according to claim 1, wherein, in said third step, said gate electrode is formed at the position between said source and drain regions over said semiconductor substrate with said multilayer film being interposed between said gate electrode and said source and drain regions.

3. The method according to claim 1, wherein, in said first step, after said impurities are introduced,

a substance having an accelerated oxidation suppressing function is subsequently introduced into said active region, and then said semiconductor substrate is annealed to form said source and drain regions.

4. The method according to claim 3, wherein said substance having an accelerated oxidation suppressing function is one selected from the group of nitrogen, carbon, and compounds containing nitrogen or carbon.

5. The method according to claim 4, wherein, as said substance having an accelerated oxidation suppressing function, nitrogen or carbon ions are implanted into said active region.

6. The method according to claim 4, wherein said substance having an accelerated oxidation suppressing function is one selected from the group of NO_2, NO, NH_3, and C_xH_y (x and y are appropriate numbers), and annealing is performed in an atmosphere of said substance to dope said active region with said substance.

7. The method according to claim 5, wherein said substance having an accelerated oxidation suppressing function is ion-implanted obliquely to a surface of said active region.

8. The method according to claim 1, wherein said first insulating film having a charge trap function is a silicon nitride film.

9. A semiconductor device comprising:

a semiconductor substrate;

source and drain regions formed in a surface layer of said semiconductor substrate;

a multilayer film formed on said semiconductor substrate between said source and drain regions, said multilayer film being made up from at least three layers, in which a first insulating film having a charge trap function is sandwiched by second and third insulating films from upper and lower sides of said first insulating film; and

a gate electrode formed on said multilayer film,

wherein said gate electrode extends between said source and drain regions over said semiconductor substrate with said multilayer film being interposed between said gate electrode and said source and drain regions, and

said source and drain regions contain a substance having an accelerated oxidation suppressing function, as well as impurities for conductivity.

10. The device according to claim 9, wherein said substance having an accelerated oxidation suppressing function is one selected from the group of nitrogen, carbon, and compounds containing nitrogen or carbon.

11. The device according to claim 9, wherein said first insulating film of said multilayer film is a capacitive insulating film, and said semiconductor substrate and said gate electrode are capacitively

coupled with each other so that said device functions as a semiconductor memory.

12. The device according to claim 9, wherein said second insulating film as the lowermost layer of said multilayer film is formed thicker at portions above said source and drain regions than at the other portions.

13. The device according to claim 12, wherein the thickness of said second insulating film above said source and drain regions falls within the range of 30 to 50 nm.

14. A method of manufacturing a semiconductor device comprising:

a semiconductor substrate;

source and drain regions formed in a surface layer of said semiconductor substrate;

a multilayer film formed on said semiconductor substrate between said source and drain regions, said multilayer film being made up from at least three layers, in which a first insulating film having a charge trap function is sandwiched by second and third insulating films from upper and lower sides of said first insulating film; and

a gate electrode formed on said multilayer film,

said method comprising the steps of:

introducing impurities into a surface layer in an active region of said semiconductor substrate;

annealing said semiconductor substrate to form

said source and drain regions; and

forming said multilayer film.

15. The method according to claim 14, wherein said gate electrode is formed at the position between said source and drain regions over said semiconductor substrate with said multilayer film being interposed between said gate electrode and said source and drain regions.

16. The method according to claim 14, wherein, after said impurities are introduced, a substance having an accelerated oxidation suppressing function is subsequently introduced into said active region, and then said semiconductor substrate is annealed to form said source and drain regions.

17. the method according to claim 16, wherein said substance having an accelerated oxidation suppressing function is one selected from the group of nitrogen, carbon, and compounds containing nitrogen or carbon.

18. The method according to claim 17, wherein, as said substance having an accelerated oxidation suppressing function, nitrogen or carbon ions are implanted into said active region.

19. The method according to claim 17, wherein said substance having an accelerated oxidation suppressing function is one selected from the group of NO_2, NO, NH_3, and C_xH_y (x and y are appropriate numbers), and annealing is performed in an atmosphere

of said substance to dope said active region with said substance.

20. The method according to claim 18, wherein said substance having an accelerated oxidation suppressing function is ion-implanted obliquely to a surface of said active region.

21. The method according to claim 14, wherein said first insulating film having a charge trap function is a silicon nitride film.